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Block Image Simulation for the Analysis of Full TFT-LCD Panel

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In this paper, we propose a novel simulation scheme, which we call "block image simulation," for the image analysis of a full thin film transistor liquid crystal display (TFT-LCD) panel. The proposed approach makes it possible to estimate viewable image for varying conditions as well as electrical characteristics of a TFT-LCD panel covering all the pixels. We also propose a compact circuit model for a TFT-LCD pixel, which accounts for the parasitic capacitors present between the neighboring gate and data lines and voltage-dependent liquid crystal (LC) pixel capacitance. In this work, we also report our successful simulation study on an exemplary 10.4 inch SVGA (800 × 600) LCD panel in terms of crosstalk, flickers, shading, and gray scale error.

Keywords: crosstalk; electrical characteristics; flickers; gray scale error; LC pixel capacitance; parasitic capacitors; shading; TFT-LCD

I. INTRODUCTION

TFT-LCD has been broadening its application to a wide-screen TV on the wall as well as for a display monitor of laptop and desktop

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computers. In order to employ a TFT-LCD for TV application, there are many technical issues to be resolved such as fast response time, wide viewing angle, brightness, short selected row-line time, and so forth. In order to devise a high-performance pixel structure, design engineers rely on a numerical simulator when they need to estimate optical characteristics like contrast ratio, voltage dependence of light transmission, time dependence of director distribution with applied voltage, and so forth [1].

Recently, it is considered that the simulation of an image characteristics of a whole display panel is very crucial as the panel size becomes wider and wider. Since the bus for gate and pixel electrode gets longer, the optical characteristics of the whole TFT-LCD panel is quite different from the expectation unless the parasitic capacitance and resistance between the electrode lines. In order to figure out the influence of the parasitic parameters on the image performance of the TFT-LCD panel, for instance, crosstalk, shading, and grey-scale errors, and flickers, we propose a novel scheme "block image simulation (BIS) method."

II. SIMULATION APPROACH

In Figure 1 is shown a schematic block diagram demonstrating a simulation procedure used in this work. To implement an equivalent circuit

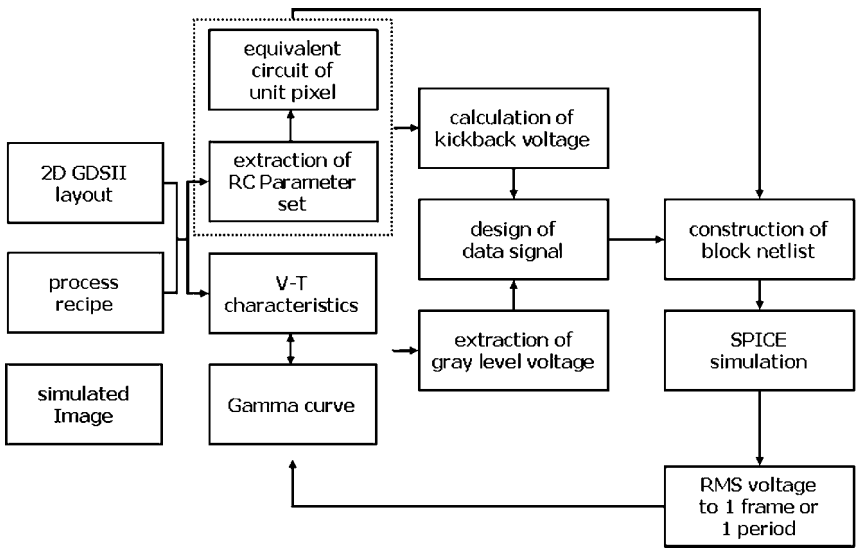

FIGURE 1 A schematic block diagram demonstrating a simulation procedure.

for full TFT-LCD panel, we need to take values for TFT parameters, capacitances, resistances, and optic characteristics including V-T curve and gamma curve of a particular pixel under investigation. Those parameters were taken through numerical simulation of a TFT- LCD pixel with a 3D finite element method (FEM) simulator, TechWiz LCD, which is available in the software market [1].

Thereafter, a gray level voltage is extracted for a particular image (for instance, SVGA 800×600) by referring to a V-T curve and a gamma correction curve which have been calculated at the previous step of a numerical calculation with a FEM solver. Now a kick-back voltage is calculated from the equivalent circuit of a pixel and a data signal is designed for a particular mode of frame inversion from the calculated kick-back voltage and the gray-level voltage. It should be also noted that the pulse width of gate and data signal is determined by the size of the panel as well as the signal frequency.

Referring to Figure 1, we should note that the kick-back voltage of a pixel is calculated from the equivalent circuit of a pixel prior to the step of calculating the data signal. Finally, a SPICE net list is constructed for the whole block for image simulation by repeating the equivalent circuit and taking the parasitic resistances and capacitances along the bus line for gate and data signals. To simulate the entire SPICE net list for the whole 800×600 panel, however, an enormous CPU time as well as huge memory is required. To overcome the issue of expensive CPU time with huge memory requirement, we devised a block image simulation (BIS) scheme. In the BIS scheme, the upper-level SPICE net list is divided into many small-size lower-level net lists. In this study, we constructed 600 net lists for the SPICE simulation with equivalent circuits of pixel arrays, which corresponds to one gate line, and lumped RC model for data lines. The pixel employed in this work is an MVA cell for 10.4″ TFT-LCD panel with a pixel size of 88×264 micrometers.

For modeling the liquid crystal (LC) capacitance of a pixel, a voltage dependent model was employed as illustrated in Figure 2. For modeling a thin-film transistor, the level 40 from the HP a-Si model was employed [2,3]. In Table 1 is shown a list of capacitance values employed in this work. The parametric values of the capacitances illustrated in Table 1 were obtained from the numerical simulation by TechWiz LCD [1].

It is assumed that the time duration of each frame is 16.7 ms while the pulse widths of a gate and data signals are 23.31 and 26.83 microsecond (μs), respectively. The root-mean-squared (RMS) value of a pixel voltage is obtained and then converted to an image data through the mapping of V-T and gamma curves. An equivalent circuit of a unit

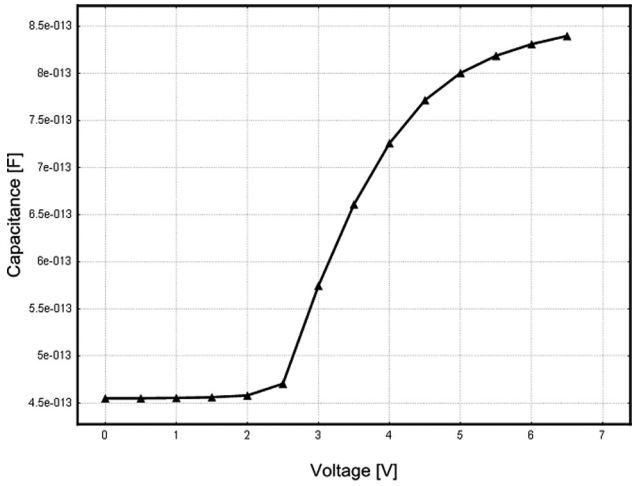

FIGURE 2 A voltage dependent model for the liquid crystal (LC) capacitance of a pixel.

pixel with adjacent gate and data line is illustrated in Figure 3. During the circuit simulation, the gate resistance was chosen to be 2 and 8 ohms while the data line resistance being 4.8 and 28.2 ohms.

III. RESULTS AND DISCUSSION

Figure 4 is an original reference image with 800×600 size having 8-bit color. The image quality of Figure 4 is SVGA while the gray-level of R, G, and B is 256. From the reference image shown in Figure 4, a gray-level was extracted from the V-T curve and a gamma correction curve.

In Figures 5(a) and 5(b) are shown the gamma correction curve and V-T curves employed in this study. As we mentioned earlier, these curves were extracted from the numerical simulator, TechWiz LCD.

In this work, it is assumed that the gate line resistance for the worst case simulation was chosen to be 8 ohms. Figure 6 exhibits the

TABLE 1 A List of Capacitance Values Employed in this Work

Capacitor	Capacitance [pF]	Capacitor	Capacitance [pF]
C_{st}	0.60657	C_{gd1}	0.01222
C_{dc1}	0.00715	C_{dc2}	0.00715
C_{dp1}	0.00515	C_{dp2}	0.00515
C_{gp1}	0.02425	C_{gp2}	0.02425

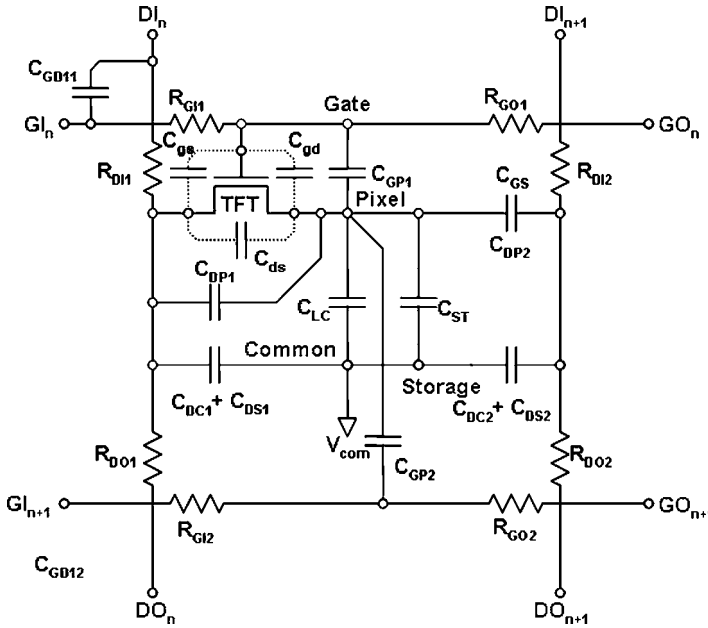

FIGURE 3 An equivalent circuit of a unit pixel with adjacent gate and data line.

FIGURE 4 An original reference image with 800 × 600 size having 8-bit color.

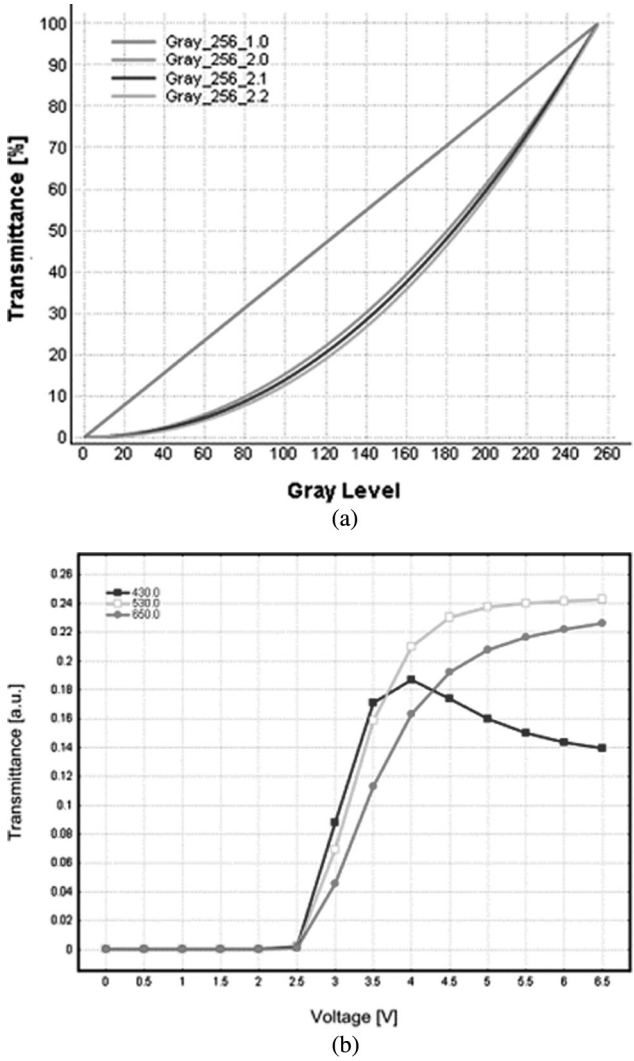

FIGURE 5 (a) V-T curve and (b) gamma curve used in this work.

simulated image taking into account all the resistance and capacitances in the model for the worst case. In this simulation, the frame inversion by column was assumed. The gate voltage ranges from −6 to 27 V while the data voltage varies between 0 and 13 V. The kick-back voltage was calculated to be 0.8 V and the common voltage was set 5.5 V.

FIGURE 6 The simulated image taking into account all the resistance and capacitances in the model for the worst case.

Referring to Figure 6, we can observe the shading effect and gray scale error induced by gate line delay in the simulated image of the panel. Furthermore, a vertical line crosstalk induced by driving with column line inversion is visible if we take a careful look at the simulated image. Though the flicker is not visibly depicted here, the effects due to data line delay are not vividly observed in the simulated image. Referring to Figure 6, the gray scale error is clearly depicted from the 1200-th pixel to the last pixel, which seems to be due to the gate line delay.

We know that the delay time of lumped RC model can be approximately expressed as the following:

$$T_m \approx mRCN^2 \tag{1}$$

where R and C represent gate line resistance and capacitance, respectively, of a unit pixel. Here N is the number of pixels, and m is a coefficient [4]. The value of m here is derived from the SPICE simulation. With the BIS approach, a limited delay time of the gate line should be no greater than 3.2 μs. From the equation (1), the m value is then 1.023, which implies that the resistance is less than 2.5 ohms.

Figure 7 exhibits a simulated image when the gate line resistance is assumed to be 2 ohms with keeping other parameters unchanged. Referring to Figure 7, we can not observe a significant effect of the gate line delay. Vertical line crosstalk seems to be alleviated with comparison to the image illustrated in Figure 6. The simulation reveals

FIGURE 7 A simulated image when the gate line resistance is assumed to be 2 ohms with keeping other parameters unchanged.

that the image quality can be adjusted either by the magnitude of the metal line or the species of material of the row-line interconnection, as mentioned earlier. A visual characteristic of the simulated image is shown in Figure 7.

As the number of pixel is increased, the gray scale error tends to be more pronounced due to the fact that the worst case panel has a greater gate line resistance than the improved panel. It is expected that the

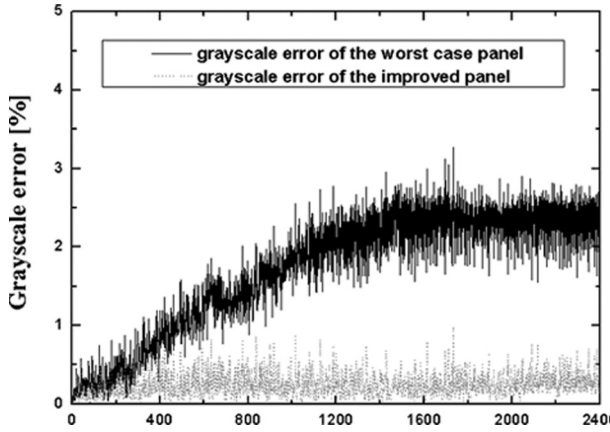

FIGURE 8 A schematic diagram illustrating the fluctuation caused by crosstalk.

panel has a negligible display distortion because gray scale error is less than 1%. In Figure 8 is shown a schematic diagram illustrating the fluctuation caused by crosstalk. Gray scale maps illustrating the differences of RMS voltages between odd and even frames are shown in Figure 9(a) and 9(b).

Referring to Figures 9(a) and 9(b), we find that there exists relatively a significant difference in the RMS pixel voltages for a bright color image while the reverse is true for a dark image. Our simulation

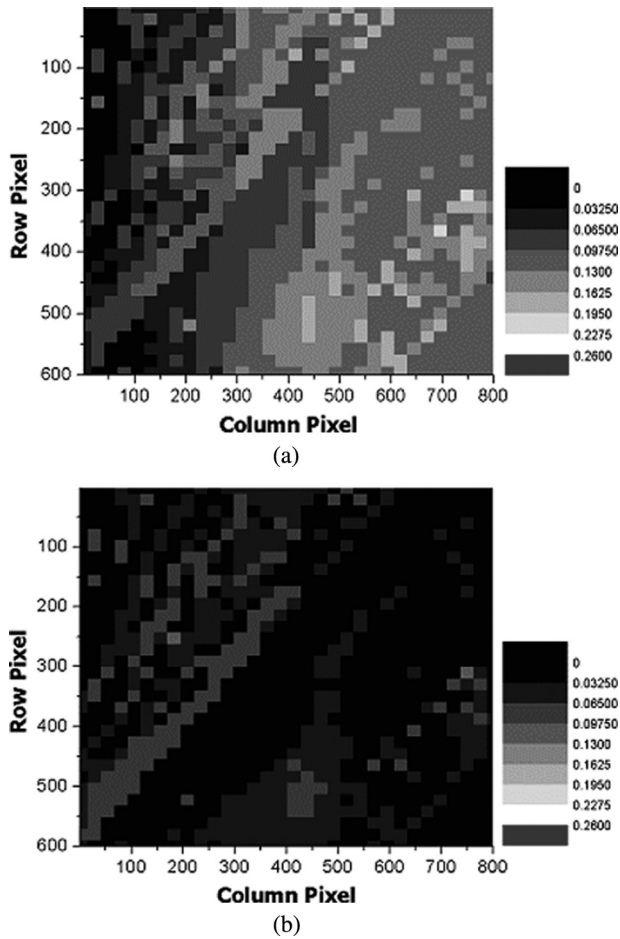

FIGURE 9 Gray scale maps illustrating the differences of RMS voltages between odd and even frames from (a) the worst case panel and (b) the improved panel.

revealed that the pixel voltages at odd and even frames are asymmetric, while flickers are caused by those differences. The differences among each frame are usually the larger with the number of pixel. Consequently, flickers are found in the worst case panel rather than the improved panel. It is expected that flickers are well observed at dark areas of the image due to the influence of gamma correction.

IV. CONCLUSION

We present a novel image simulation scheme, so-called block image simulation (BIS) method, which makes it possible to perform a full analysis of TFT-LCD panel and observe various phenomenological effects influencing the image quality of the TFT-LCD. In this paper, electrical characteristics for 10.4″ SVGA TFT-LCD panel have been simulated by considering the voltage-dependent LC pixel capacitances and parasitic capacitances induced by adjacent gate and data lines. The simulation provides the visualization and also the valid prediction for the improvement of TFT-LCD panel. Various effects due to RC delay such as flickers were theoretically investigated, which implies a clue to design issue. The proposed technique can be applied to all types of TFT-LCD panel as well as MVA mode investigated in this work.

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